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EXAMINER	
FOSTER, DAVID A	

ART UNIT	PAPER NUMBER
2835	11

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/158,616	Applicant(s) Dalal et al.
	Examiner David Foster	Art Unit 2835

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-7 and 9-52* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-7, 9, 10, 12-33, and 35-52* is/are rejected.

7) ☒ Claim(s) *11 and 34* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☒ The proposed drawing correction filed on *Sep 30, 2000* is: a) ☒ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

A MULTI-LEVEL ELECTRONIC PACKAGE

AND METHOD FOR MAKING SAME

Dalal et al.

Allowable Subject Matter

1. Prosecution on the merits of this application is reopened on claims 1-7, 9, 10, 12-26, 27, 28, 29-32, 34, 35 and 36-52 considered unpatentable for the reasons indicated below:

A subsequent prior art search has shown additional art which addresses the non-allowability of this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 5-7, 9, 10, 12-26, 29-33 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al. (5,570,274).

Reference claim 1 Saito et al. discloses package for containing electronic components, the package comprising: a first circuitized card; a second circuitized card (see elements 1 in Figure

9); an interposer interposed between the first and second circuitized cards (see elements 4 located between elements 1 in Figure 9), the interposer comprising a circuitized card (see column 3,lines 13-17), and having an opening (Figure 3A), the opening of the interposer and the first and second circuitized card forming a cavity for containing at least one electronic component (the cavity is represented by the space where elements 2 in Figure 9 are mounted), wherein the first circuitized card has a bottom surface and there is at least one component mounted to the bottom surface (see elements 2 mounted to the bottom element 1).

Reference claim 2. Saito et al. disclose a package of claim 1 wherein the interposer, first circuitized card and second circuitized card **act** as a Faraday shield for electronic components placed inside the cavity (Figure 3B, items 1 and 10).

Reference claim 5. Saito et al disclose a package of claim 1 wherein the opening is square and is in the approximate center of the interposer (Figure 3A).

Reference claim 6. Saito et al. disclose a package of claim 1 wherein the interposer is electrically and physically connected to the first and second circuitized cards (Figure 3B).

Reference claim 7. Saito et al. disclose a package of claim 1 wherein the first circuitized card has a top surface and there is at least one component mounted to the top surface (Figure 3B).

Reference claim 9. Saito et al. disclose a package of claim 1 wherein the second circuitized card has a top surface and there is at least one component mounted to the top surface (Figure 9, item 2).

Reference claim 10. Saito et al. disclose a package of claim 1 wherein the second circuitized card has a bottom surface and there is at least one component mounted to the bottom surface (Figure 9).

Reference claim 12. Saito et al. disclose a package of claim 1 wherein the second circuitized card has a bottom surface and the bottom surface has a ball grid array allowing connection to a system board (Figure 9).

Reference claim 13. Saito et al. disclose a package of claim 6 wherein the first circuitized card and interposer are connected through surface mount or through-hole technologies and wherein the interposer and the second circuitized card are connected through surface mount or through-hole technologies (Figure 3B and column 5, line 20).

Reference claim 14. Saito et al. disclose a package of claim 13 wherein the interposer and first circuitized card are connected through a ball grid array and the interposer and the second circuitized card are connected through a ball grid array (Figures 3A and 9, items 11).

Reference claim 15. Saito et al. disclose a package of claim 1 wherein the first circuitized card has a top surface and a bottom surface, the second circuitized card has a top surface and a bottom surface, and there is at least one component on the top surface of the first circuitized card, there is at least one component the bottom surface of the first circuitized card, and there is at least one component the top surface of the second circuitized card (Figure 9).

Reference claim 16. Saito et al. disclose a package of claim 1 wherein at least one component is mounted to the first circuitized card and wherein the at least one component is attached to a heat sink or pick-up plate (Figure 9, items 1 and 2).

Reference claim 17. Saito et al. disclose a package of claim 1 wherein the cavity contains at least one component (Figure 3A).

Reference claim 18. Saito et al. disclose a package of claim 17 wherein the at least one component inside the cavity is attached to a bottom surface of the first circuitized card or a top surface of the second circuitized card and wherein the at least one component is attached to the bottom surface of the first circuitized card or the top surface of the second circuitized card through surface mount attachment, direct chip attachment or through-hole attachment (Figure 9).

Reference claim 19. Saito et al. disclose a package of claim 1 wherein the first circuitized card has a top surface and there is at least one component attached to the top surface of the first circuitized card through surface mount attachment, direct chip attachment or through-hole attachment (Figure 9 and column 5, line 20).

Reference claim 20. Saito et al. disclose a package for containing electronic components, the package comprising: a first circuitized card having a top surface and a bottom surface; a second circuitized card having a top surface and a bottom surface; and an interposer having an opening, a top surface, and a bottom surface, the interposer being electrically connected to the first circuitized card and the second circuitized card through a first and second set of connections (Figure 9, items 11), the first set of connections being interposed between the bottom surface of

the first circuitized card and the top surface of the interposer, the second set of connections being interposed between the bottom surface of the interposer and the top surface of the second circuitized card, wherein the bottom surface of the second circuitized card has a third set of connections for attaching the second circuitized card to a system card, and wherein the opening in the interposer, the bottom surface of the first circuitized card and the top surface of the second circuitized card forming a cavity for containing at least one electronic component.

Reference claim 21.Saito et al. disclose a package of claim 20 wherein the cavity contains at least one electronic component (Figure 4, item 2).

Reference claim 22. Saito et al. disclose a package of claim 21 wherein the at least one component inside the cavity is attached to a bottom surface of the first circuitized card or a top surface of the second circuitized card and wherein the at least one component is attached to the bottom surface of the first circuitized card or the top surface of the second circuitized card through surface mount attachment, direct chip attachment or through-hole attachment (Figure 9, items 2 and column 5, line 20).

Reference claim 23. Saito et al. disclose a package of claim 21 wherein the first circuitized card has a top surface and there is at least one component attached to the top surface of the first circuitized card through surface mount attachment, direct chip attachment or through-hole attachment (Figure 9 items 2 and column 5, line 20).

Reference claim 24. Saito et al. disclose a package of claim 20 wherein each set of connections of the first, second, and third sets of connections is a plurality of surface mount connections, or a plurality of through-hole connections (Figure 9).

Reference claim 25. Saito et al. disclose a package of claim 24 wherein each set of connections of the first, second, and third sets of connections is a ball grid array (Figures 3A, 9, items 11.

Reference claim 26. Saito et al. disclose a package of claim 20 wherein the interposer acts as a Faraday shield for electronic components placed inside the cavity (Figure 3B, items 1 and 10).

Reference claim 29. Saito et al. disclose a package of claim 20 wherein the opening is square or rectangular and is in the approximate center of the interposer (Figure 9).

Reference claim 30. Saito et al. disclose a package of claim 20 wherein there is at least one electronic component mounted to the top surface of the first circuitized card (Figure 9).

Reference claim 31. Saito et al. disclose a package of claim 20 wherein there is at least one electronic component mounted to the bottom surface of the first circuitized card (Figure 9).

Reference claim 32. Saito et al. disclose a package of claim 20 wherein there is at least one electronic component mounted to the top surface of the second circuitized card (Figure 9).

Reference claim 33. Saito et al. disclose a package of claim 20 wherein the interposer has at least one electronic component on its surface (Figure 9).

Reference claim 35. Saito et al. disclose a package of claim 20 further comprising a third circuitized card and a second interposer having a second opening, wherein the third circuitized card, second circuitized card, and the second opening in the second interposer define a second

cavity for containing at least one electronic component, wherein the third circuitized card is electrically connected to the second interposer through a fourth set of connections, and wherein the second interposer is electrically connected to the second circuitized card through a fourth set of connections (Figure 9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (5,570,274).

Reference claims 3, 4, 27 and 28. Saito et al. do not directly disclose package of claim 2 wherein the interposer has at least one connection to at least one ground. However, Saito et al. do disclose a motherboard (Figure 3B, item 10) to which the multichip module is placed. It is well known in the art of the necessity to provide grounding to a motherboard for mechanical and electrical purposes in order to suppress EMI and proper terminations in order to avoid unwanted frequency reflections. Though Saito et al. do not specifically the technique for grounding, this does not preclude having the motherboard (Figure 3B) grounded.

Reference claims 36-53. Claims 36-53 are method claims and the method of assembly is inherently obvious in view of the apparatus rejected above.

Allowable Subject Matter

6. Claims 11 and 34 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The best art to consider with this application can be found in Czaya et al. DE 43 26 104 A1, OSAMU (JP 6-120670), Beaman et al. (5,371,654), Grabbe et al. (4,699,593), Dranchak et al. (5,953,214), Booth et al. (5,384,955), Iwasaki (5,834,848), Buckley, III et al. (5,477,082), Kim (5,978,229), Bertin et al. (5,977,640), Pasch (5,468,681), Beilin et al. (5,854,534), Chan (5,838,551) and Higgins, III (5,639,989). Czaya et al. disclose a multilayer board having components located between the layers of board, Osamu discloses a multilayer board having two or more layers having components mounted within the layers, Beaman et al. disclose a structure having two subcomponent assemblies each with a substrate and a multilevel wiring structure, Grabbe et al. disclose a chip carrier having a housing frame, contact modules and contact pads on a substrate, Dranhchak et al. disclose a dual substrate package having an intermediate connection between the substrates, Booth et al. disclose a method of replacing IC

ship package wiring having an interposing, Iwasaki et al. disclose an electronic device and semiconductor package mounted on a motherboard and a buffer layer for relieving a stress, Buckley, III et al. disclose a bi-planar multi-chip module which has a die mounted on both sides of an insulating flexible carrier, Kim discloses an apparatus and a process for mounting integrated circuit packages on circuit boards, Bertin et al. disclose a chip-on-chip component connection/interconnection for electrically connecting the fully functional chips to external circuitry, Pasch discloses a process for interconnecting conductive substrates using an interposer having conductive plastic filled vias, Beilin et al. disclose an interposer substrate for mounting an integrated circuit chip to a substrate, Chan discloses an electronic package with an electronic component mounted on a PCB or ceramic substrate wherein the component is protected by an EMI shield and Higgins, III discloses electronic components shield from electromagnetic interference (EMI) by one or more conformal layers filled with selected filler particulars for attenuating specific EMI frequencies.

action.

Any inquiry concerning to this communication or earlier communications from the Examiner should be directed to David Foster whose telephone number is (703) 308-1763. The examiner can normally be reached on Monday through Thursday and alternate Fridays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Darren E. Schuberg, who can be reached on (703) 308-4815. The fax phone number for the organization where this application or proceeding is assigned is (703)308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DAF

November 30, 2000

DARREN SCHUBERG
PRIMARY EXAMINER
Supervisory Patent